AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of designing a programmable logic device comprising the steps of:

defining modules of a circuit design comprising components of a same type;

prior to annealing the circuit design, determining a set of static shapes for ~~associated with~~ each module; [[and]]

annealing the circuit design to determine a floorplan by, at least in part,

for each module during a first iteration of annealing, selecting a ~~different~~ shape from the set of static shapes associated with the ~~corresponding to at least one~~ module and applying the selected shape to the ~~at least one~~ module[[,]]; and

for at least one module during at least one further iteration of annealing, selecting a different shape from the set of static shapes associated with the at least one module and applying the different shape to the at least one module, wherein each iteration of annealing the circuit design is evaluated according to evaluation of a cost function.

2. (Original) The method of claim 1, said defining step further comprising splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type.

Claim 3. (Cancelled)

4. (Previously Presented) The method of claim 1, said annealing step further comprising assigning modules and assigned shapes to locations on the programmable logic device.

5. (Original) The method of claim 4, said annealing step further comprising at least one of swapping locations of components of a same type that have associated grid sites, swapping two modules in a sequence pair, and switching the shape of a module from one shape in the set of shapes associated with that module to another.

6. (Original) The method of claim 4, said annealing step further comprising using bipartite matching of individual components.

7. (Original) The method of claim 4, further comprising:
identifying modules that share a timing critical path; and
moving identified modules closer to one another.

8. (Original) The method of claim 1, wherein the programmable logic device is a Field Programmable Gate Array.

9. (Previously Presented) The method of claim 1, wherein each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed macro to be placed within that module.

10. (Original) The method of claim 1, further comprising:
generating a flat placement flow for the circuit design; and
comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan.

11. (Currently Amended) A system for designing a programmable logic device comprising:
means for defining modules of a circuit design comprising components of a same type;
means for determining a set of static shapes for ~~associated with~~ each module prior to annealing the circuit design; [[and]]
means for annealing the circuit design to determine a floorplan comprising ~~by, at least in part~~,
means for, for each module during a first iteration of annealing, selecting a ~~different~~ shape from the set of static shapes associated with the ~~corresponding to at least one~~ module and applying the selected shape to the ~~at least one~~ module, and
means for, for at least one module during at least one further iteration of

annealing, selecting a different shape from the set of static shapes associated with the at least one module and applying the different shape to the at least one module, wherein each iteration of annealing the circuit design is evaluated according to evaluation of a cost function.

12. (Original) The system of claim 11, said means for defining further comprising means for splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type.

Claim 13. (Cancelled)

14. (Previously Presented) The system of claim 11, said means for annealing further comprising means for assigning modules and assigned shapes to locations on the physical device.

15. (Original) The system of claim 14, said means for annealing further comprising means for performing at least one of swapping locations of components of a same type that have associated grid sites, swapping two modules in a sequence pair, and switching the shape of a module from one shape in the set of shapes associated with that module to another.

16. (Original) The system of claim 14, wherein said means for annealing use bipartite matching of individual components.

17. (Original) The system of claim 14, further comprising:
means for identifying modules that share a timing critical path; and
means for moving identified modules closer to one another.

18. (Original) The system of claim 11, wherein the programmable logic device is a Field Programmable Gate Array.

19. (Previously Presented) The system of claim 11, wherein each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed macro to be placed within that module.

20. (Original) The system of claim 11, further comprising:

means for generating a flat placement flow for the circuit design; and

means for comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan.

21. (Currently Amended) A machine readable storage, having stored thereon a computer program having a plurality of code sections executable by a machine for causing the machine to perform the steps of:

defining modules of a circuit design comprising components of a same type;

prior to annealing the circuit design, determining a set of static shapes for ~~associated with~~ each module; [[and]]

annealing the circuit design to determine a floorplan by, at least in part,

for each module during a first iteration of annealing, selecting a ~~different~~ shape from the set of static shapes associated with the ~~corresponding to at least one~~ module and applying the selected shape to the ~~at least one~~ module, and

for at least one module during at least one further iteration of annealing, selecting a different shape from the set of static shapes associated with the at least one module and applying the different shape to the at least one module, wherein each iteration of annealing the circuit design is evaluated according to evaluation of a cost function.

22. (Original) The machine readable storage of claim 21, said defining step further comprising splitting modules into sub-modules, wherein at least one of the sub-modules consists of components of a same type.

Claim 23. (Cancelled)

24. (Previously Presented) The machine readable storage of claim 21, said annealing step further comprising assigning modules and assigned shapes to locations on the physical device.

25. (Original) The machine readable storage of claim 24, said annealing step further comprising at least one of swapping locations of components of a same type that have associated grid sites, swapping two modules in a sequence pair, and switching the shape of a module from one shape in the set of shapes associated with that module to another.

26. (Original) The machine readable storage of claim 24, said annealing step further comprising using bipartite matching of individual components.

27. (Original) The machine readable storage of claim 24, further comprising:
identifying modules that share a timing critical path; and
moving identified modules closer to one another.

28. (Original) The machine readable storage of claim 21, wherein the programmable logic device is a Field Programmable Gate Array.

29. (Previously Presented) The machine readable storage of claim 21, wherein each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed macro to be placed within that module.

30. (Original) The machine readable storage of claim 21, further comprising:
generating a flat placement flow for the circuit design; and
comparing the annealed circuit design with the flat placement flow to determine a measure of quality for the determined floorplan.